

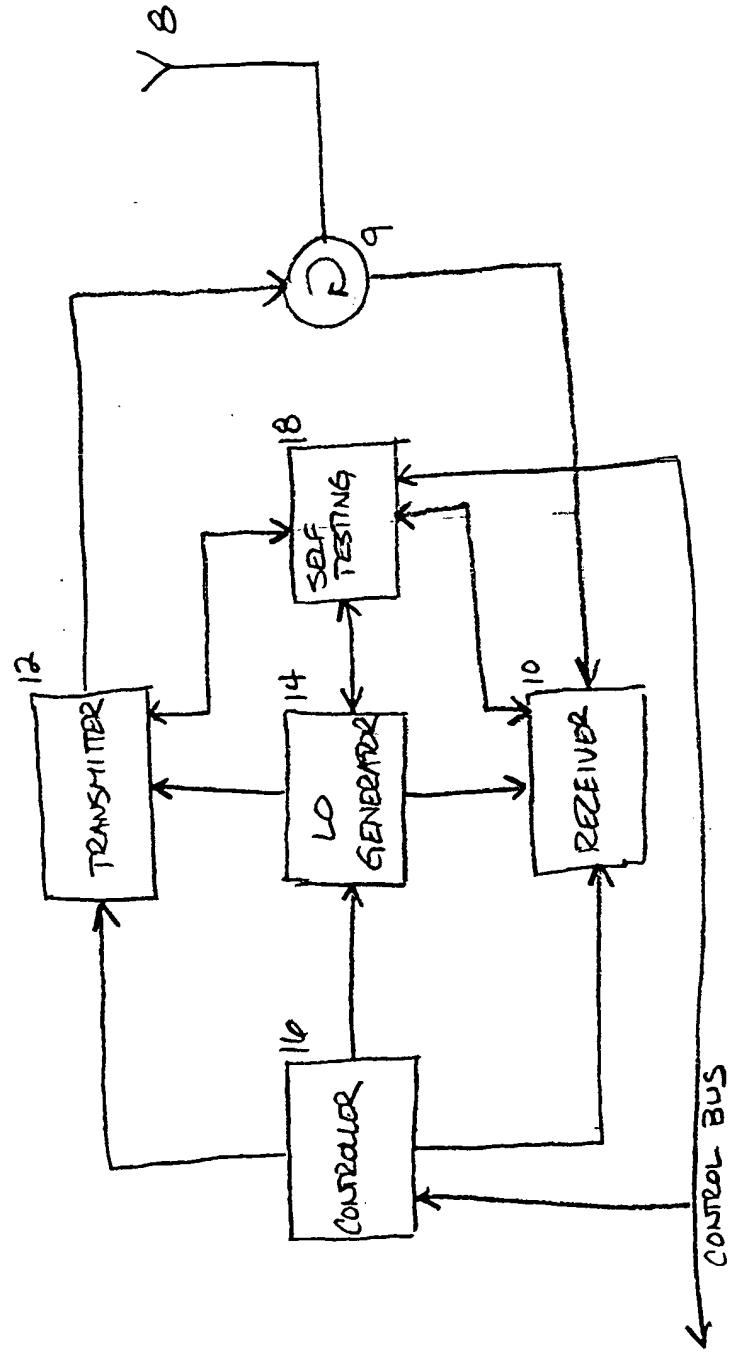
[illegible]

Fig. 1

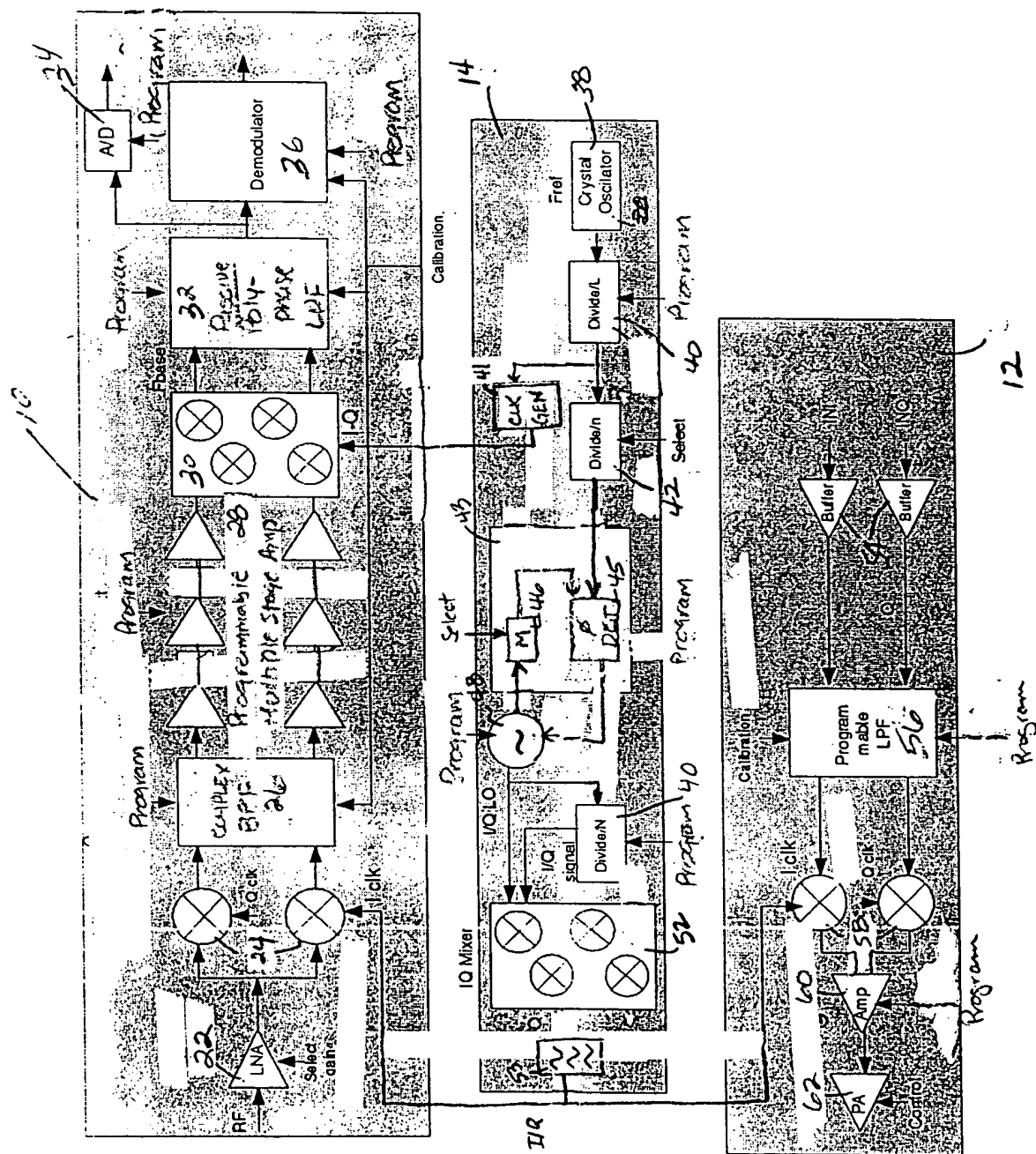
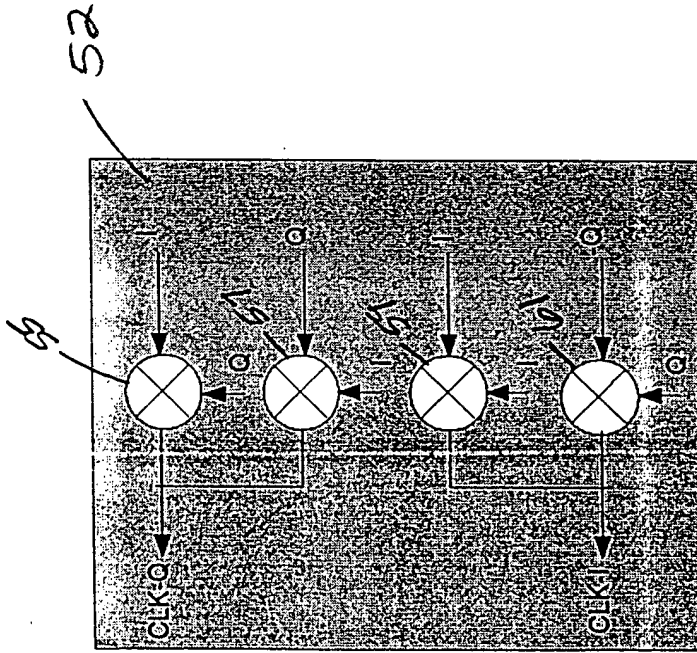
[illegible]

Fig. 2

[illegible]

५६३

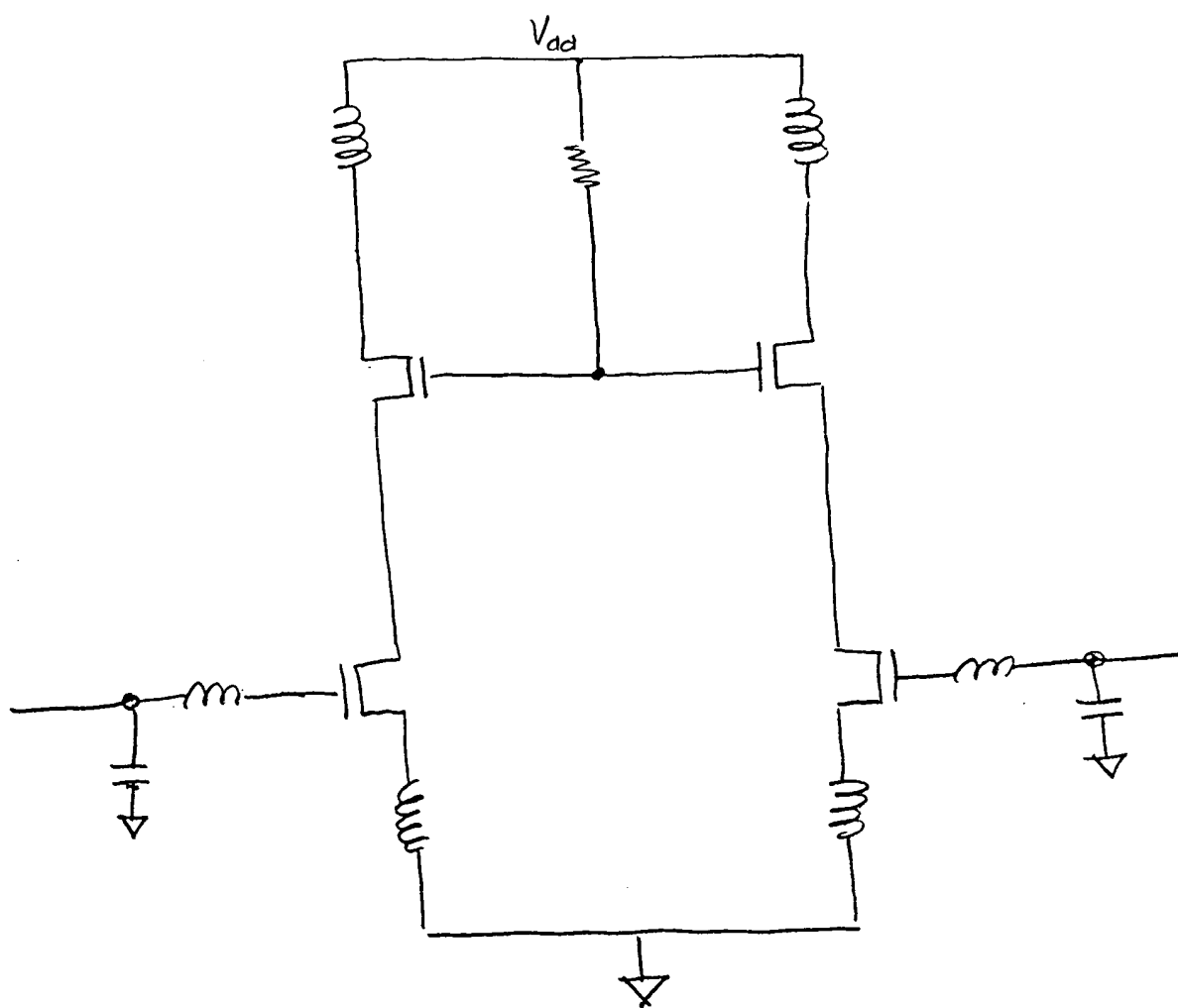
[illegible]

FIG. 4 (a)

FIG. 4

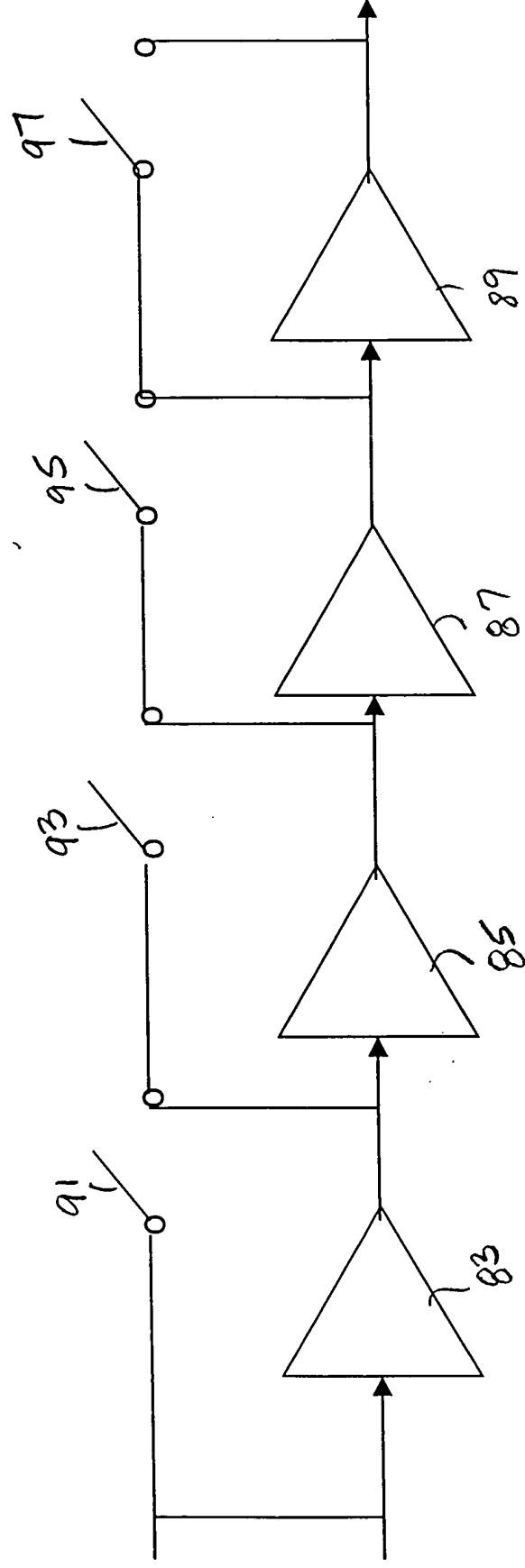


FIG. 5

FIG. 6

A hand-drawn graph of the magnitude response $|H(\omega)|$ versus angular frequency ω for a second-order low-pass filter. The curve is a downward-opening parabola. The peak value is labeled $122 A$. The half-power frequency is marked as $2RC$, with a corresponding value of $A/\sqrt{2}$ on the y-axis. The -3dB frequency is marked as $2Q/RC$, with a corresponding value of $A/(1+(4Q)^2)$ on the y-axis. The graph is labeled with handwritten notes: 126 and 124 .

FIG. 7

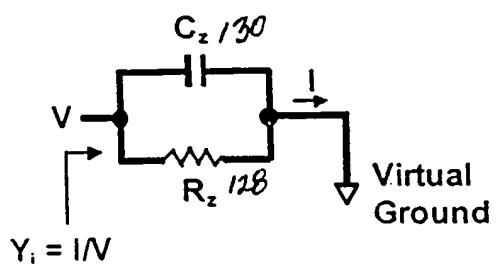


FIG. 8

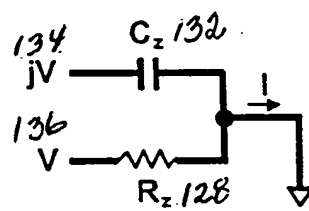


FIG. 9

FIG. 10

000001-19920900

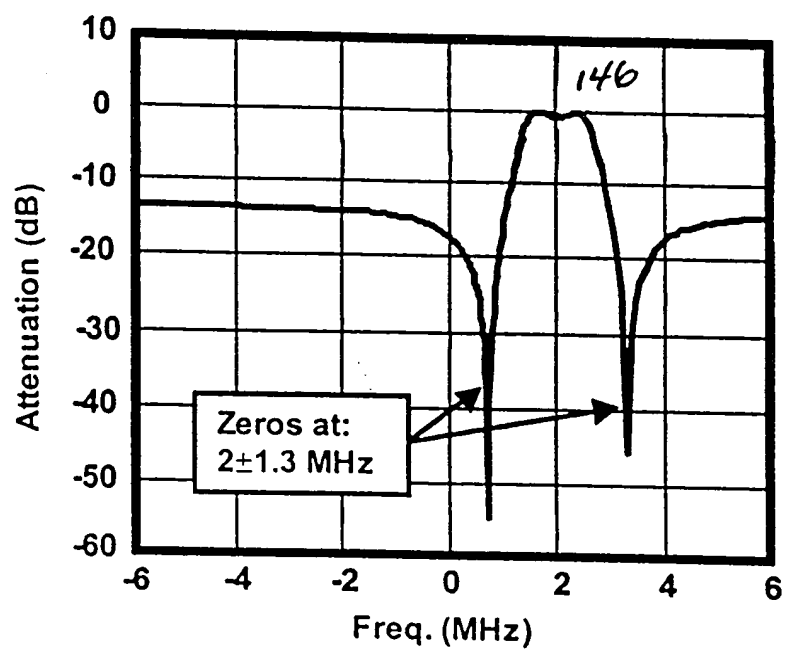


FIG. 11

Diagram of a 4-bit parallel adder using four 1-bit full adders. The inputs are A_4, A_3, A_2, A_1 and B_4, B_3, B_2, B_1 . The outputs are S_4, S_3, S_2, S_1 . The carry chain starts with $C_0 = 0$ and produces C_1, C_2, C_3, C_4 .

FIG. 12(b)

000000-19920000

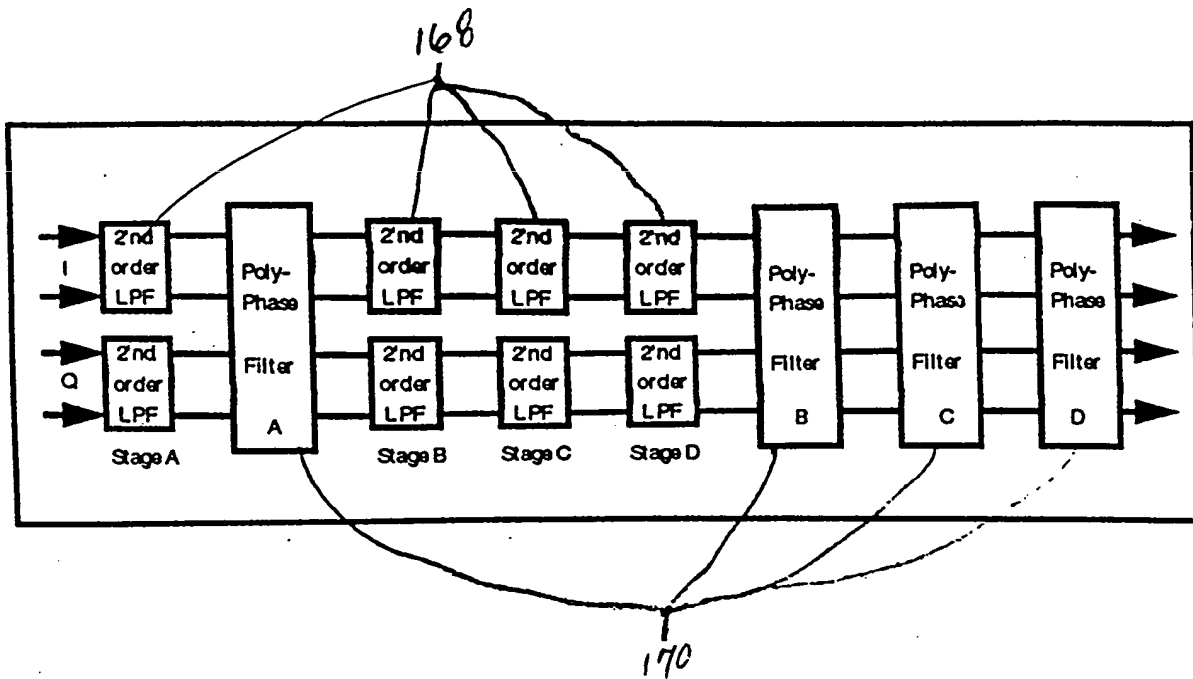


FIG. 13

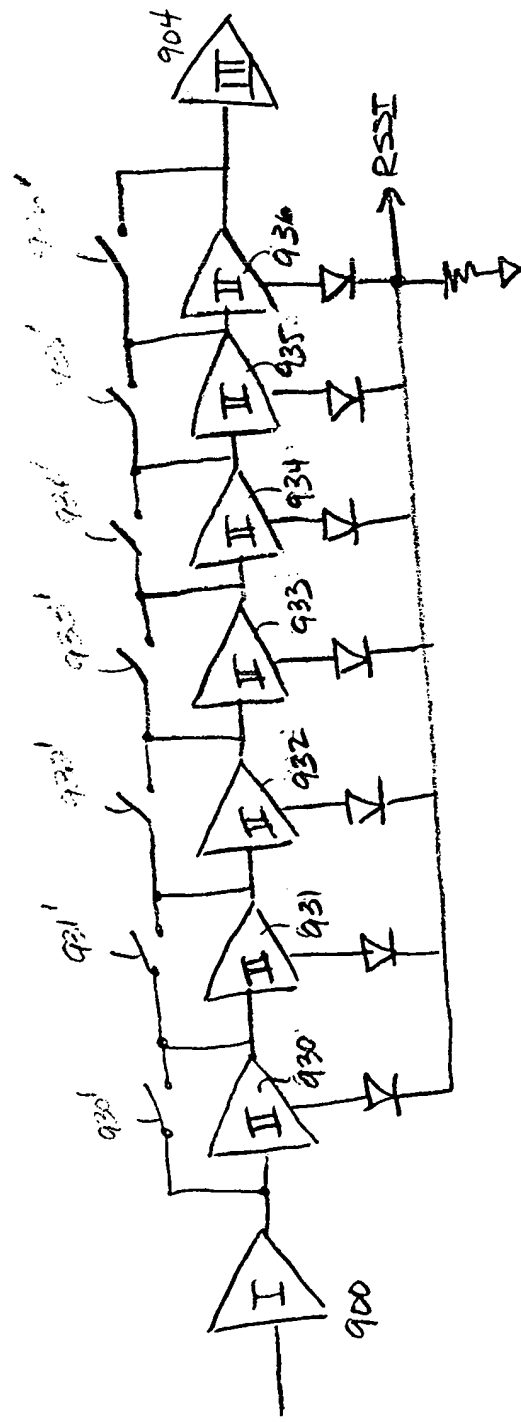


FIG. 14

FIG. 15

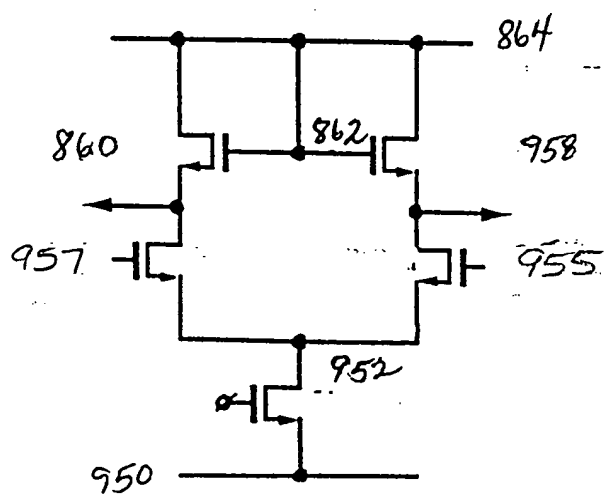


FIG. 16(a)

000001-10100

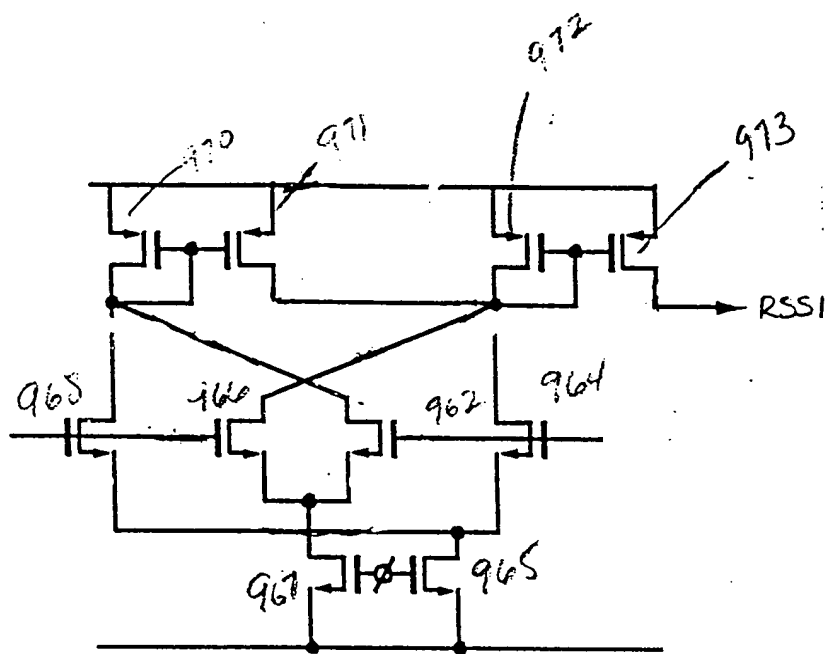
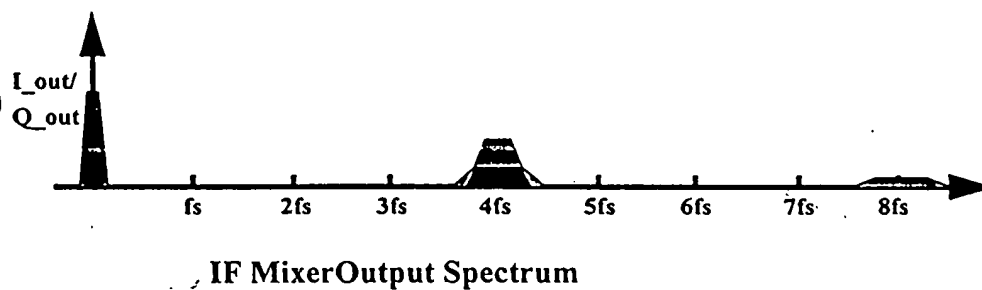
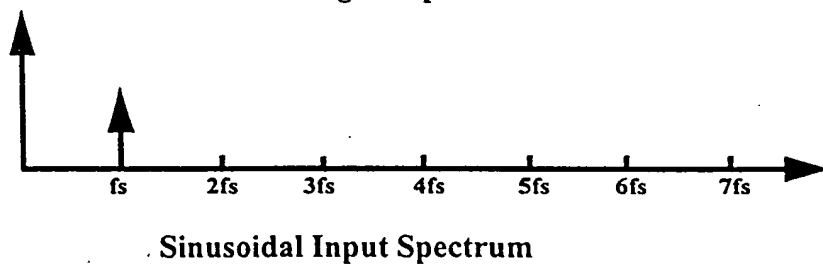
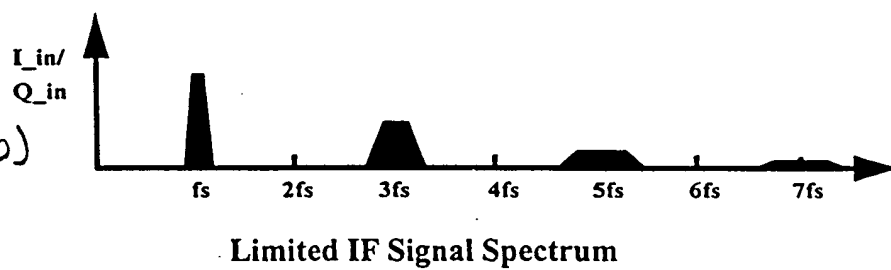
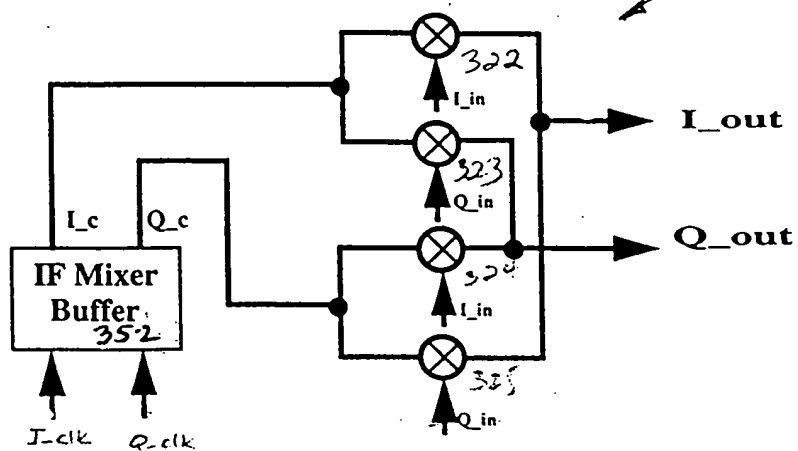


FIG. 16(b)



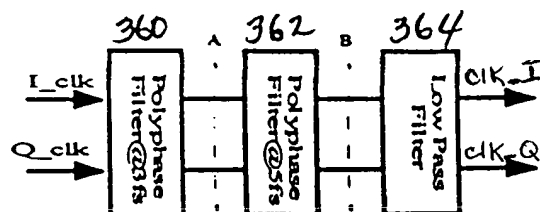


FIG. 18

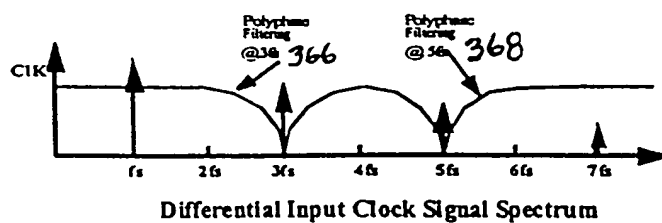


FIG. 19(a)

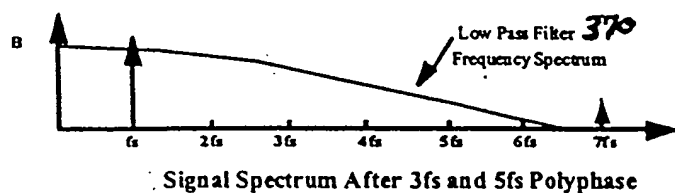


FIG. 19(b)

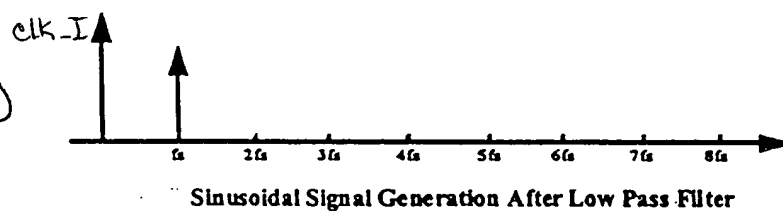
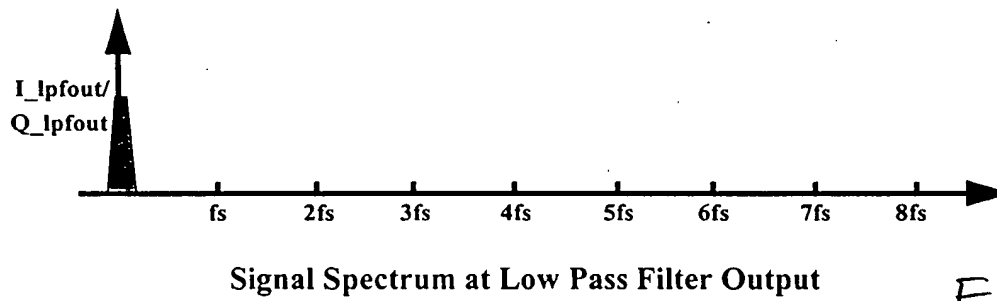
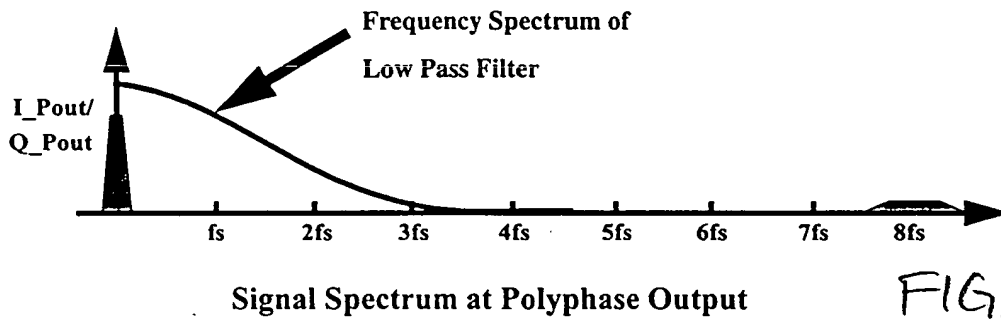
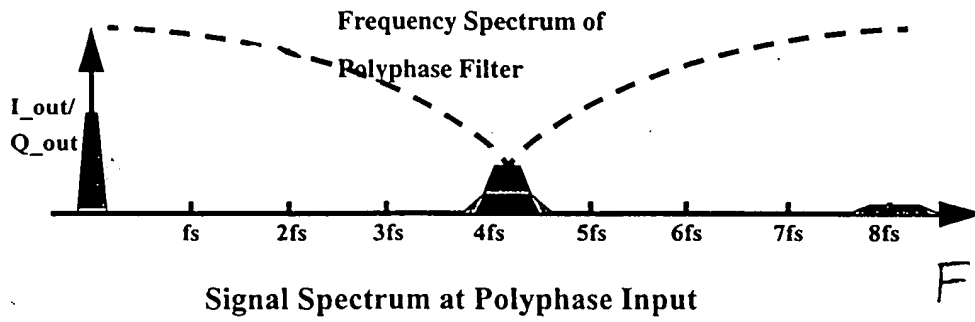
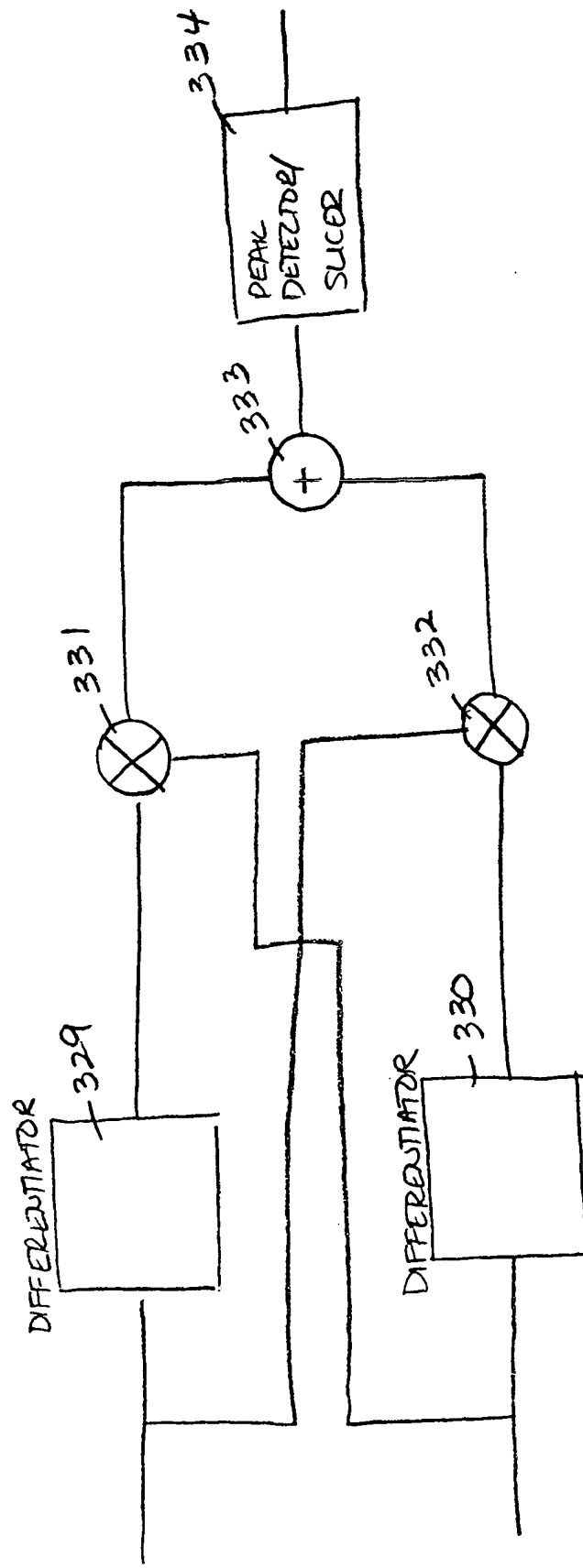


FIG. 19(c)



Abstract



F16. 21

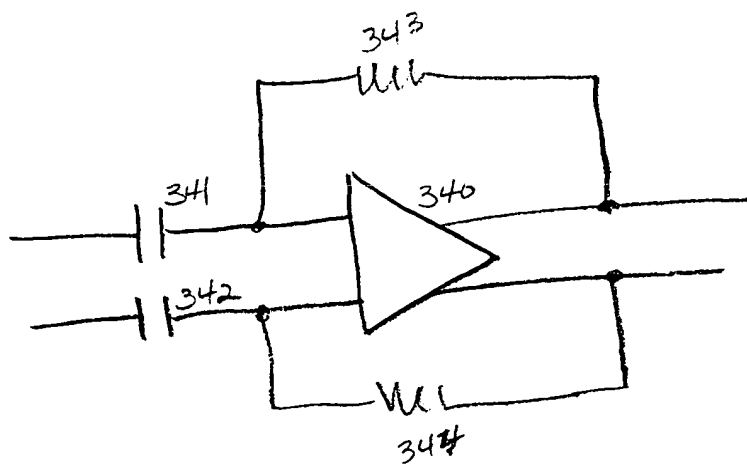
[illegible]

FIGURE 22

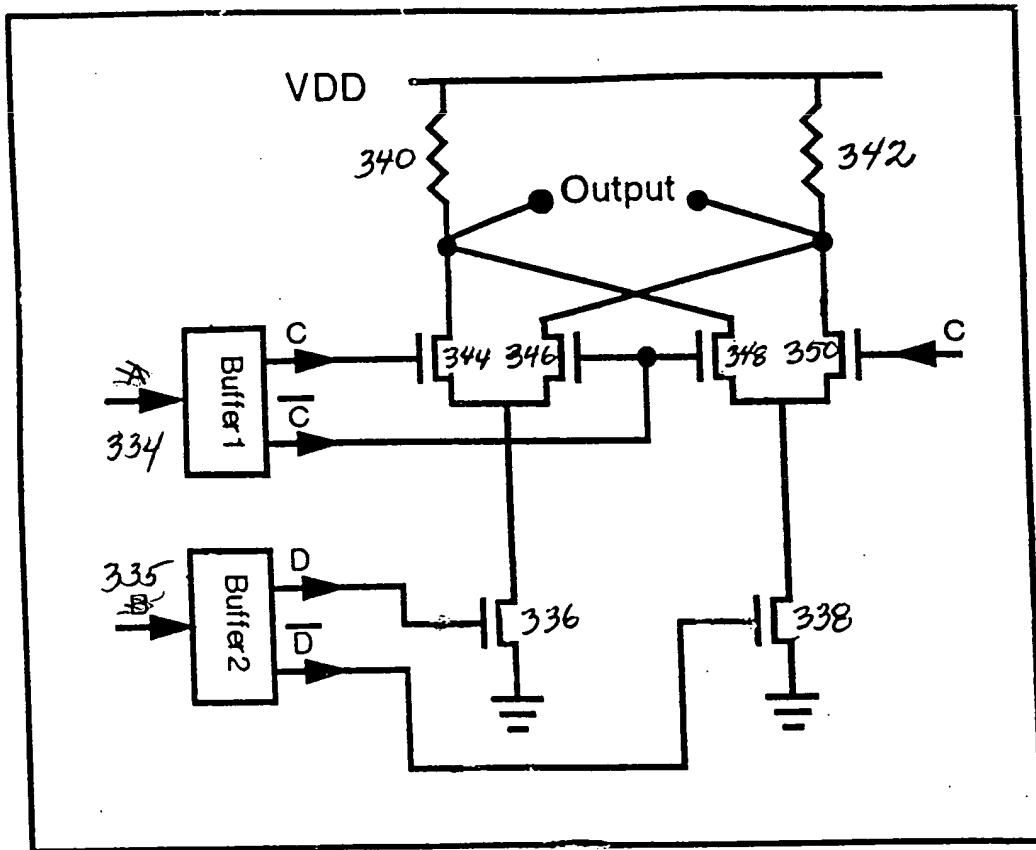


FIG. 23

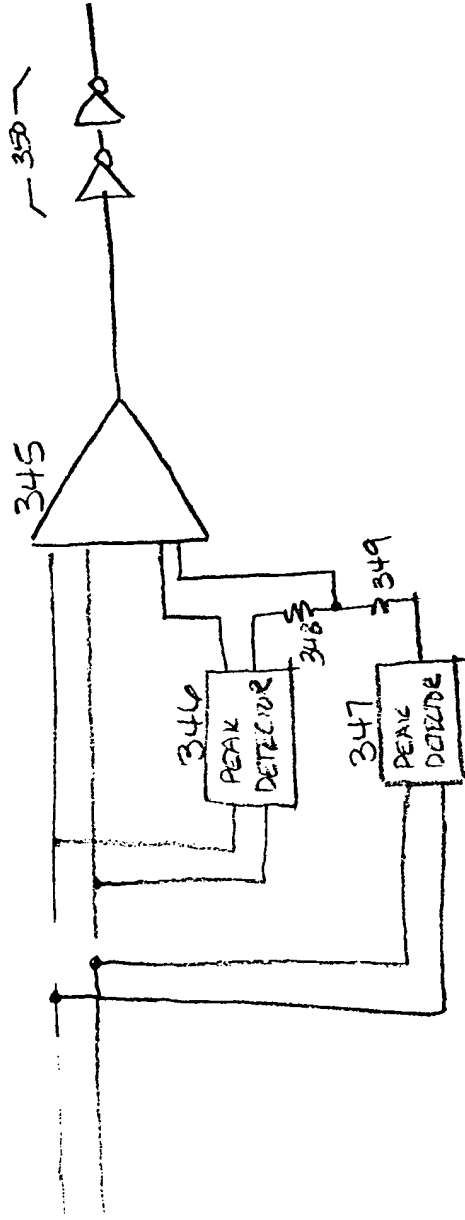


FIGURE 24

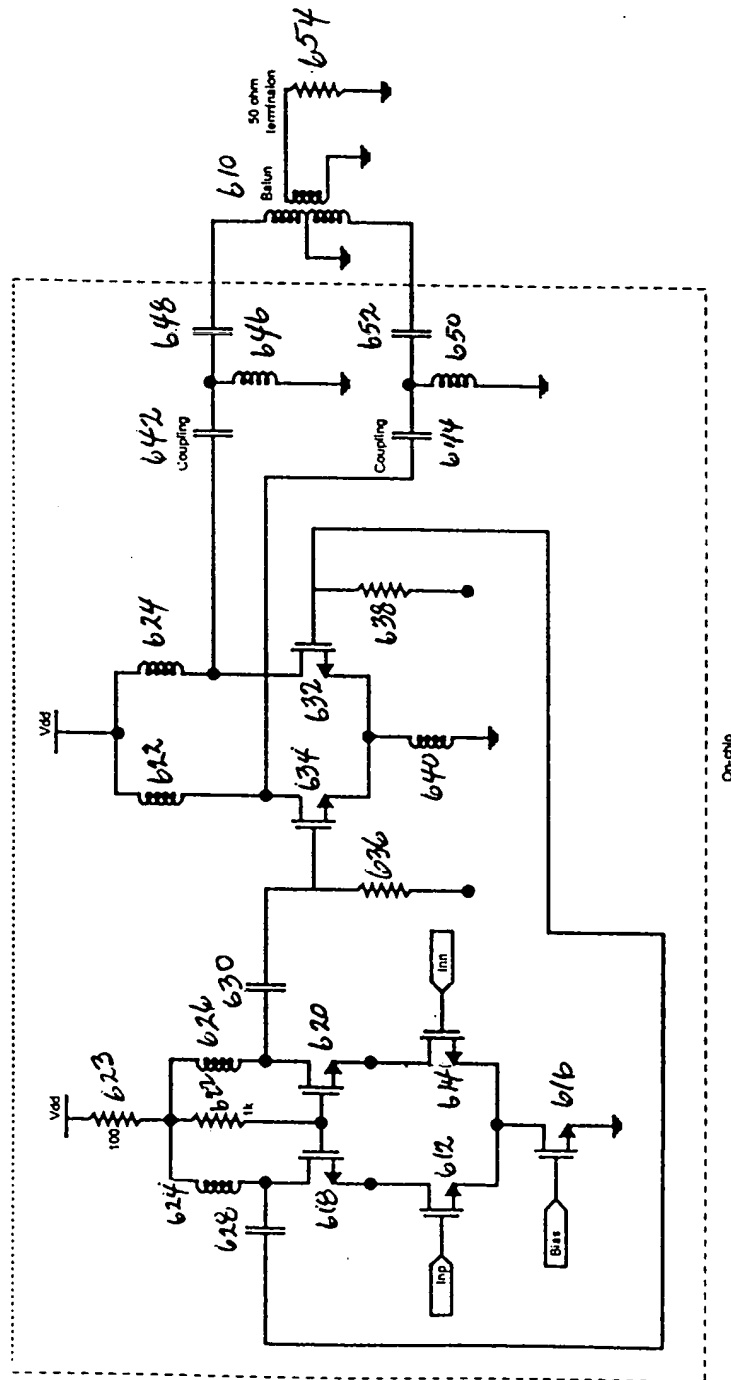


FIG. 25

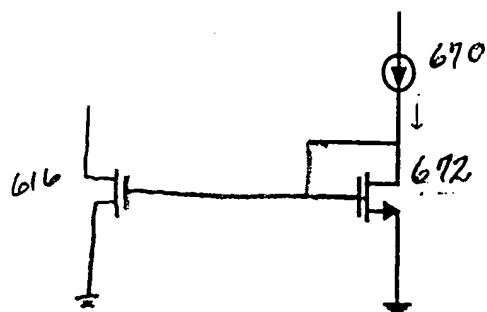


FIG. 27

FIG. 28

FIG. 29

000001-101000

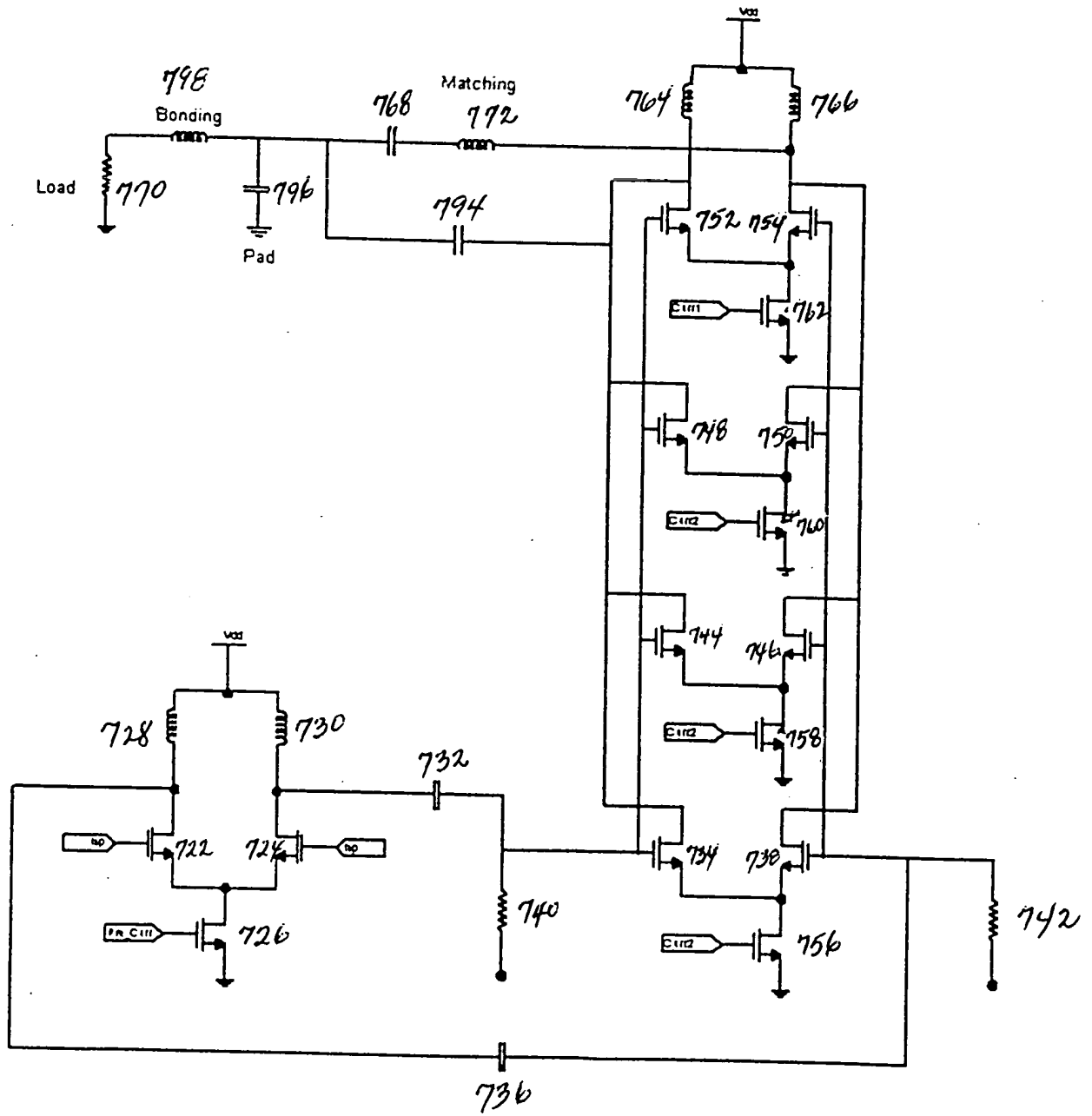


FIG. 30

FIG. 32

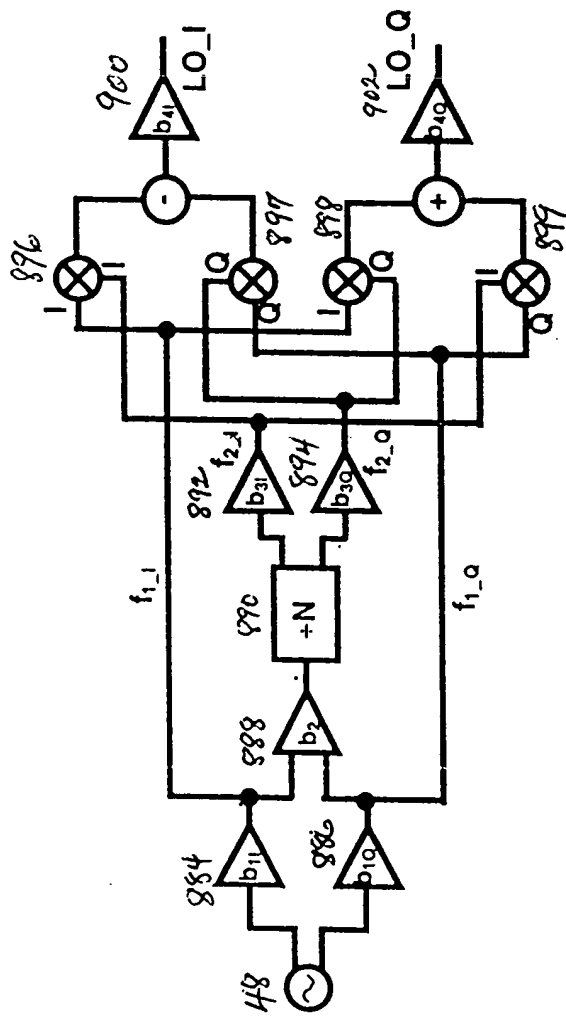


FIG. 33

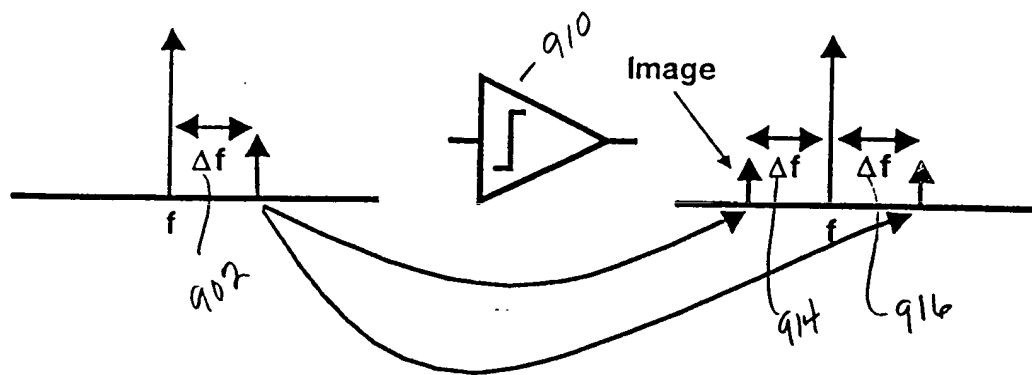
[illegible]

FIG. 33(a)

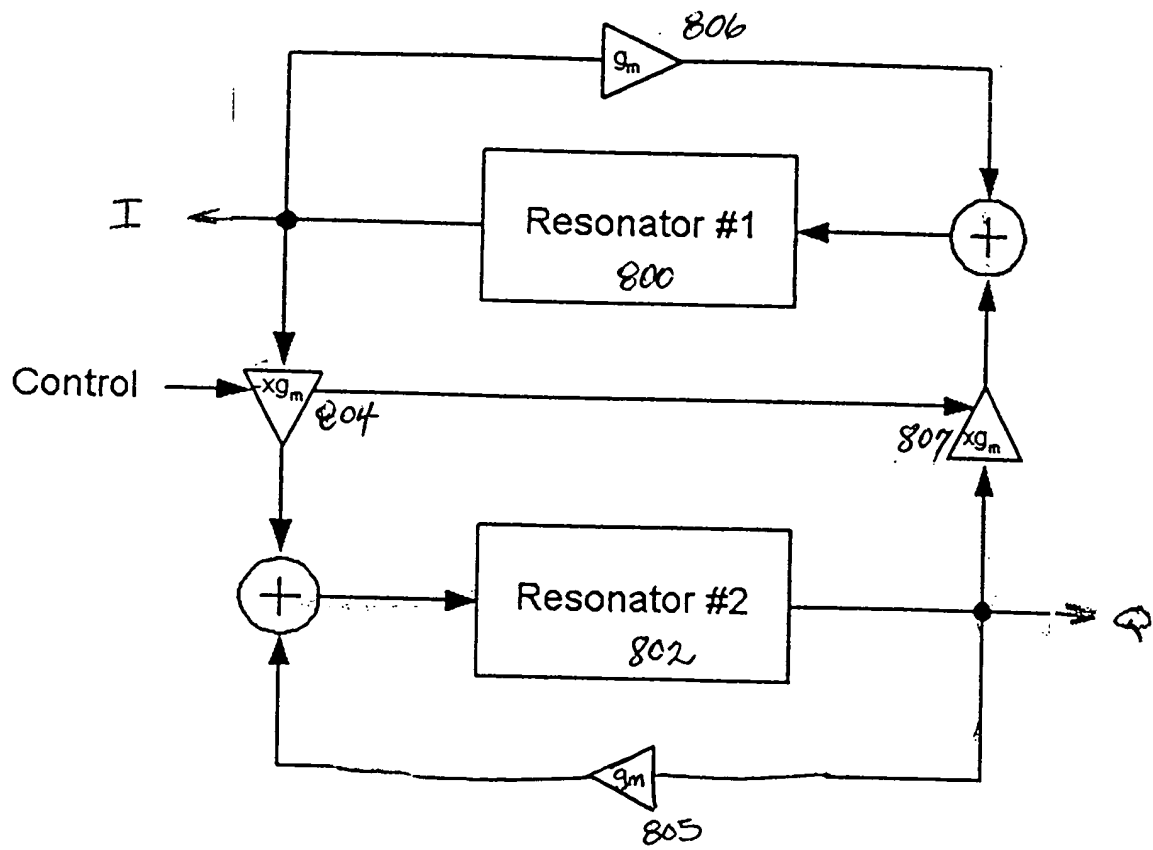


FIG. 34

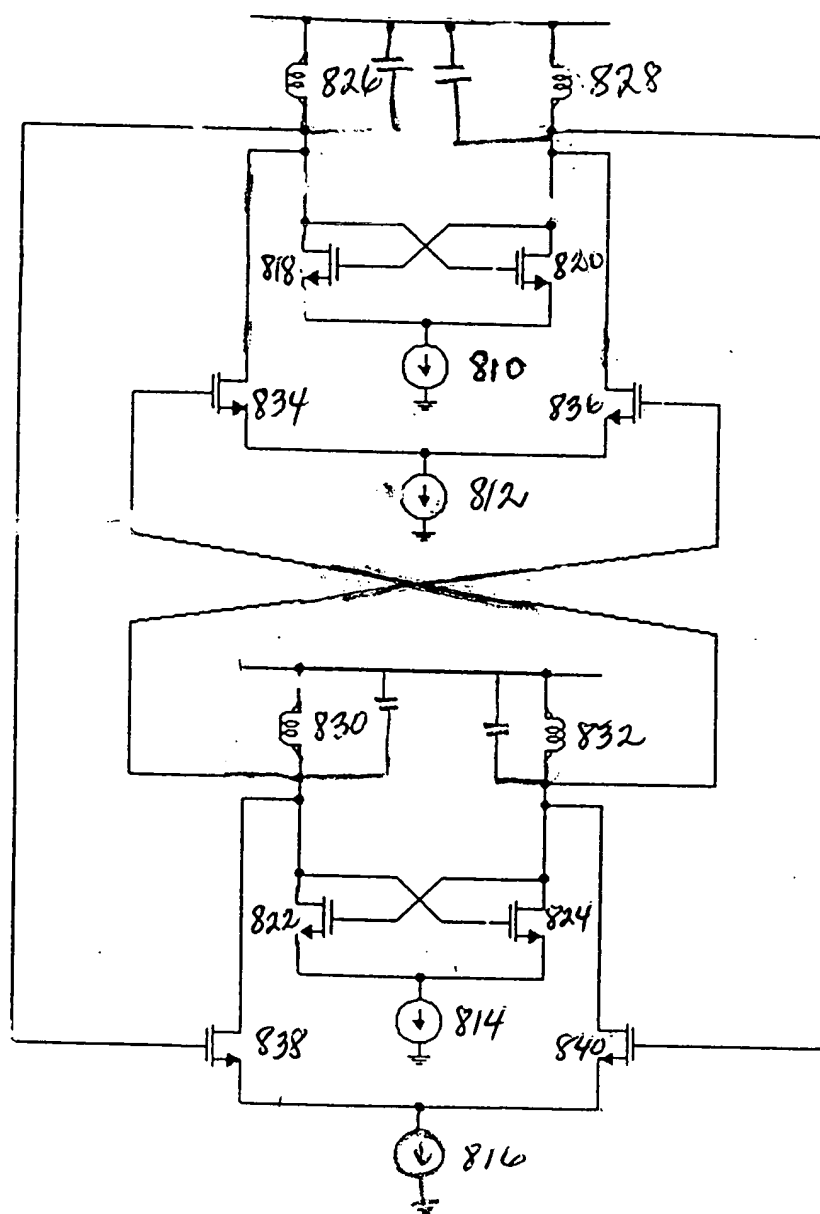
[illegible]

FIG. 35

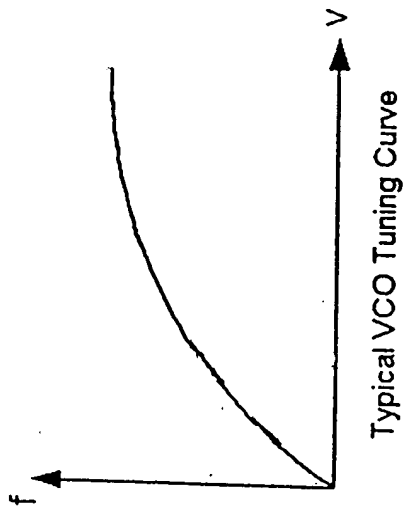


FIG. 36(a)

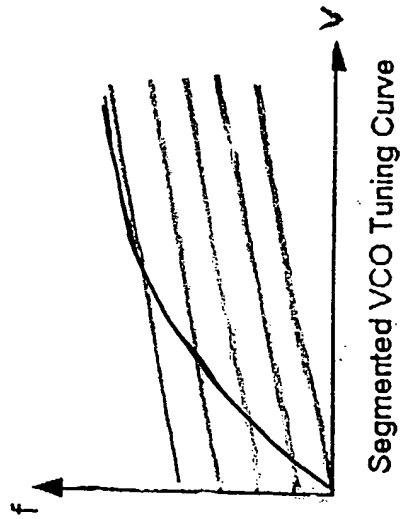


FIG. 36(b)

[illegible]

FIG. 27(a)

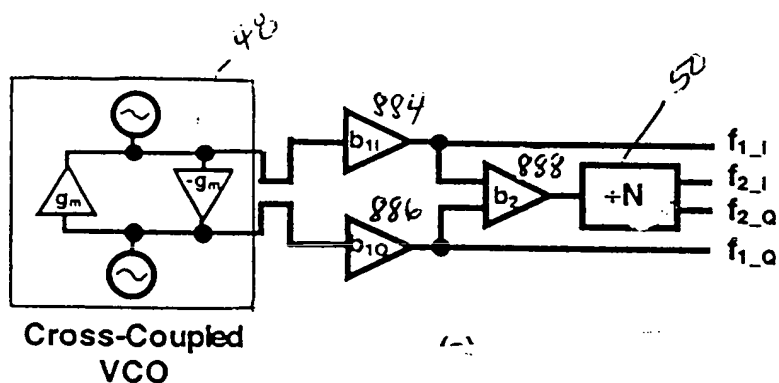
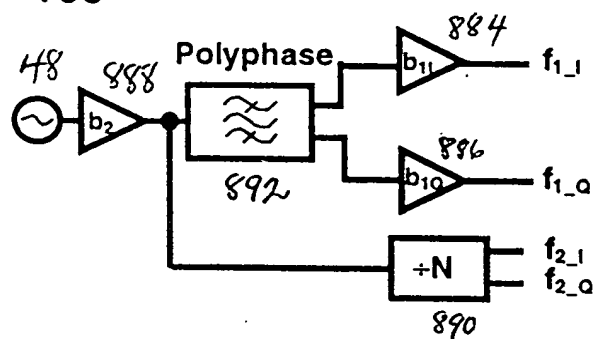


FIG. 37(b)



FROM
EXTERNAL
PROCESSING
DEVICE

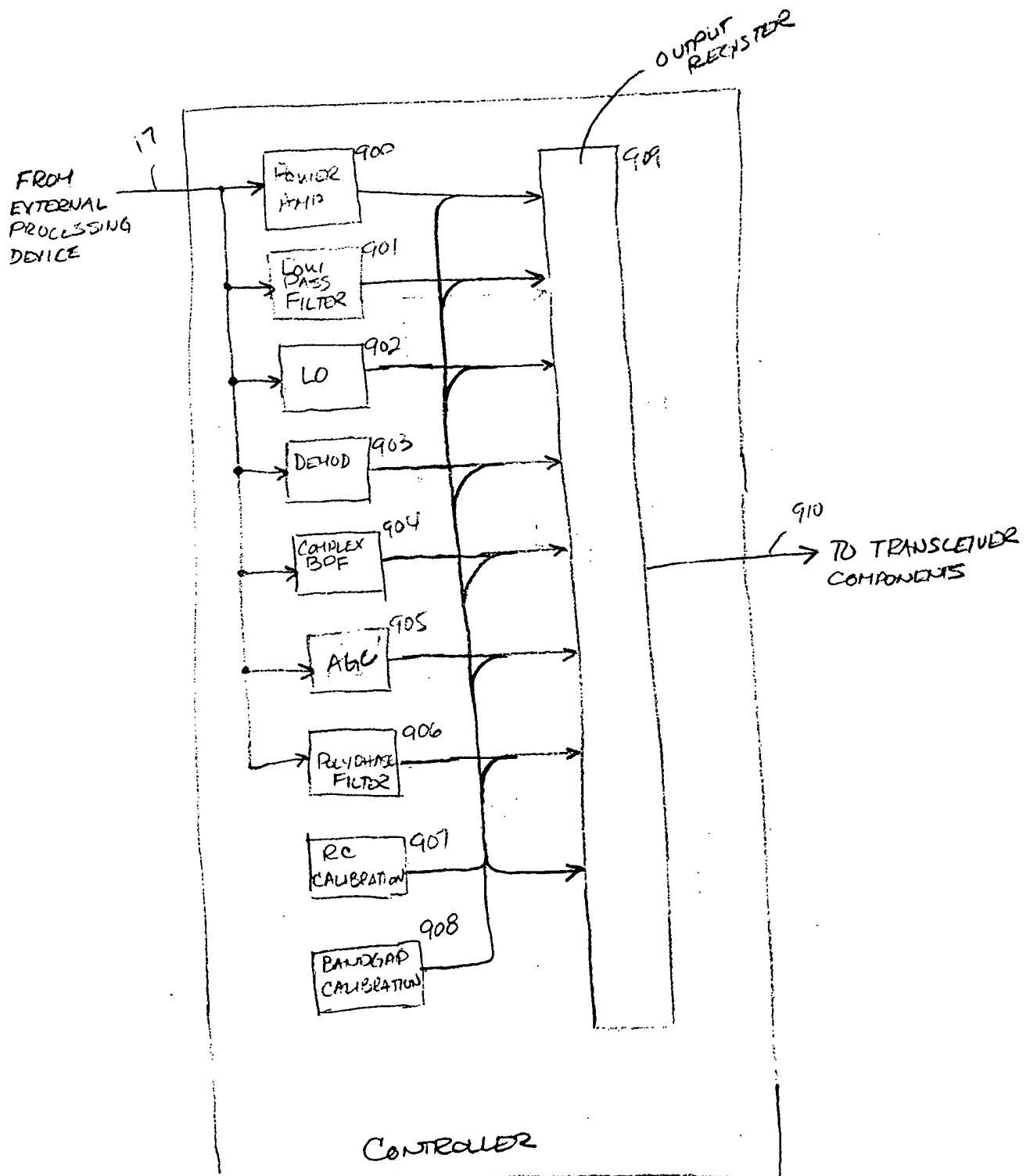


FIGURE 38

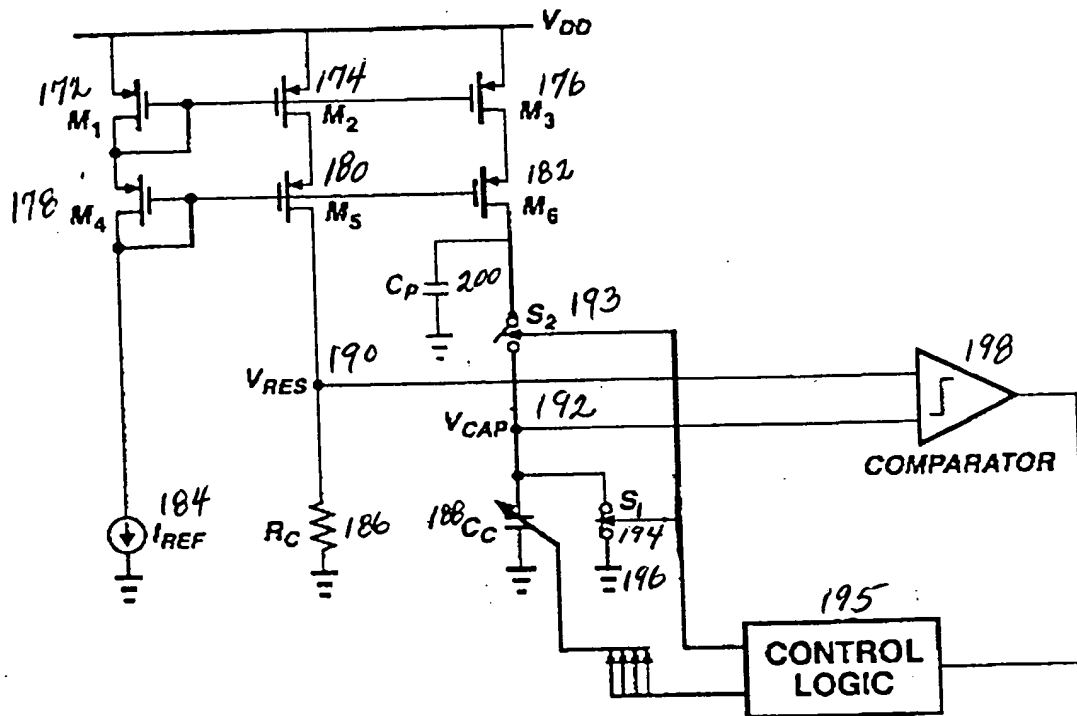
[illegible]

FIG. 39

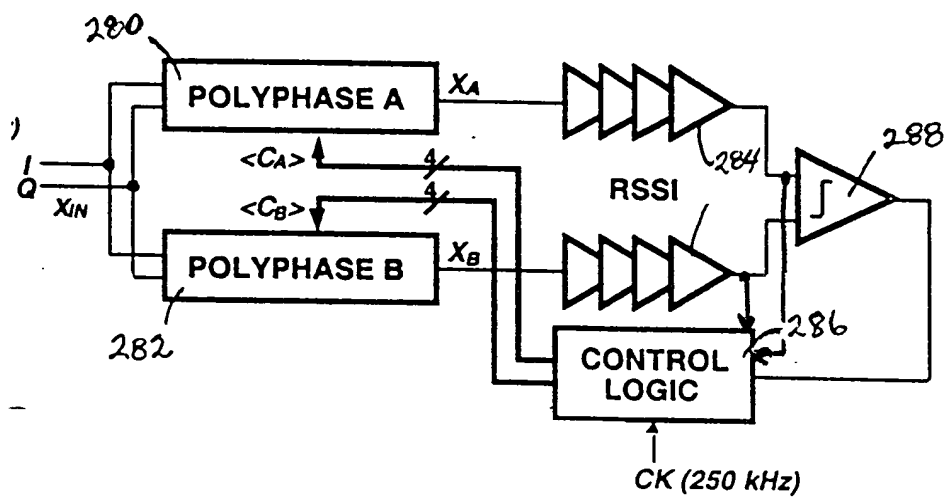
[illegible]

FIG. 40

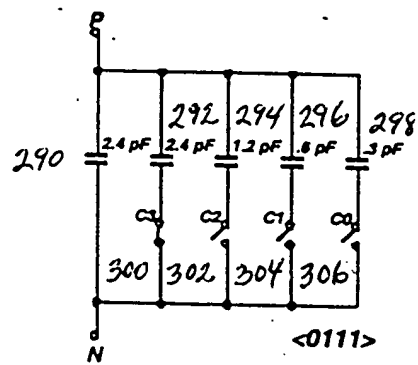
[illegible]

FIG. 41

[illegible]

FIG. 42

FIG. 43

000001-10100

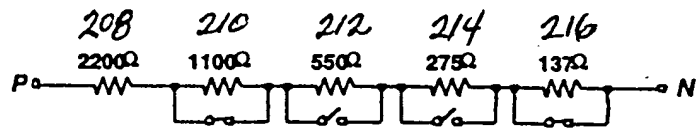


FIG. 44

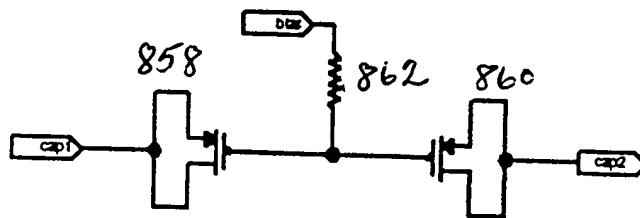


FIG. 45

00592561-101800

Hand-drawn schematic of a PA/LNA switch circuit. The circuit features two MOSFETs, 642 and 644, controlled by a common gate signal. MOSFET 642 is in series with the PA (off) path, while MOSFET 644 is in series with the LNA (on) path. The PA path includes a coupling capacitor 646, a matching network with capacitors 648 and 650, and a 50 ohm antenna. The LNA path includes a coupling capacitor 644 and a bypass capacitor 652. Waveforms show the input signal and the output of the PA and LNA stages.

FIG. 47